AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph [0041] with the following paragraph rewritten in amendment format:

Referring now to FIG. 2, the line cache interfaces 52-1 and 52-2 of the ~~host and~~ servo and host CPUs 50-1 and 50-2, respectively, are connected by a line cache arbitration device 100 to the line cache 58. While host and servo processors are shown, other types of processors may be used. The line cache arbitration device 100 resolves line cache conflicts that occur between the CPUs 50-1 and 50-2, as will be described more fully below. A priority scheme may be employed. For example, in disk drive applications, the servo CPU ~~50-2~~ 50-1 may have priority over the host CPU ~~50-1~~ 50-2, although other priority schemes may be employed.

Please replace Paragraph [0043] with the following paragraph rewritten in amendment format:

The line cache arbitration device 100 allows both the ~~host and~~ servo and host CPUs 50-1 and 50-2 to retrieve data and/or code from the line cache 58. In some implementations, the line cache 58 includes 4 lines of 8 x 32 bits, although other numbers of cache lines and line sizes/widths can be used. The device switch 64 allows the line cache 58 to be used for both the buffer memory 79 and the flash memory 86. The direct interface 74 can be maintained for data access without flushing out the contents of the line cache 58. The IRd/Prog interface 84 allows data to be directly read from or written to the flash memory 86. A cache address tag that is used by the CPU and the line cache is a virtual address for both the buffer and flash memories, as will be

described below. Cache performance is related to the number of integrated cache lines. Two small cache RAMS are less effective than one larger one. In addition, flash and buffer memory execution usually originate from separate routines, therefore concurrent execution occurs infrequently.

Please replace Paragraph [0045] with the following paragraph rewritten in amendment format:

Referring now to FIG. 3, virtual dual CPU addressing space for the embodiment of FIG. 2 is shown. A host CPU address 110 generated by the host CPU ~~50-1~~ 50-2 is input to the line cache arbitration device 100. A servo CPU address 114 generated by the servo CPU 50-1 is also input to the line cache arbitration device 100. The arbitration device 100 selects one of the requests when two occur at the same time. The host and servo CPU addresses 110 and 114 include a first portion 120 containing a CPU address. The addresses 110 and 114 also include a memory select portion 122 containing one or more bits for selecting the target memory. For example, the first portion 120 may include bits [15:0] and the memory select portion may contain bit [16]. A first state of the memory select portions 122 and 126 selects the buffer memory 79 and a second state selects the buffer flash memory 86. The arbitration device 100 outputs a translated address 130 or 130' to the line cache 58.